UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,743	12/26/2001	Hiroki Kanai	500.36683CX1	2044

7590 04/02/2002

ANTONELLI, TERRY, STOUT & KRAUS, LLP
Suite 1800
1300 17th Street
Arlington, VA 22209

EXAMINER
MCLEAN, KIMBERLY N

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 04/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,743	KANAI ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11 and 12* is/are rejected.

7)☒ Claim(s) *1,2,7 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09,181,676* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Preliminary Amendment submitted, Information Disclosure Statement and the Application submitted on December 26, 2001.

Drawings

2. Figure 13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/181,676, filed on October 29,1998.

Specification

4. The disclosure is objected to because of the following informalities: .

The disclosure appears to be a literal translation into English from a foreign document and is replete with grammatical and idiomatic errors. The Applicants, or their attorneys or agents, are urged to reexamine the specification for any mistakes of a clerical or idiomatic or grammatical or typographical nature or of minor character. Appropriate correction is required.

Claim Objections

5. Claims 1-2 and 12 are objected to because of the following informalities: . Appropriate correction is required.

Claim 1, Line 6 states, "memory controller further comprising". This should state, "memory controller comprising".

Claim 1, Line 9 delete ";" after wherein.

Claim 1, Line 9 change "judging" to "judgement".

Claim 1, Line 10, "an most probable" should state "a most probable".

Claim 1, Line 12 delete "a".

Claim 1, Line change "buffer memory" to "buffer".

Claim 1, Line 13 delete "," after memory.

Claim 2, Line 3 and Line 5 and Claim 12, Lines 6-7, change "the access" to "the memory access".

Claim 2, Lines 5-6 appears to have missing words. Should this state, "..fails to hit data within said buffer, is controlled to.." ?

Claim 2, Line 5 change "whereas" to "wherein".

Claim 12, Line 13 change "an judgement" to "a judgement".

The Applicants, or their attorneys or agents, are urged to reexamine the claims for any mistakes of a clerical or idiomatic or grammatical or typographical nature or of minor character. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 5 recites the limitation "said access unit" in Line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

10. Claims 1, 5, 8 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanabe (USPN: 5,752,272).

Regarding claim 1, Tanabe discloses an information processing system (Figure 4) comprising a processor (Figure 4, Reference 3); a memory (Figure 4, Reference 5); and a memory controller connected with the processor via a first bus (BC) and connected with the memory via a second bus (RB) for controlling the memory (Figure 4, Reference 1); wherein the memory controller comprises a buffer (Figure 4, Reference 29R), a control circuit (Figure 4, comprised of References 21 and 23), an access judging circuit (Figure 4, Reference 30), wherein the control circuit estimates a most probable address to be accessed next in the memory (C 10, L 19-50), and wherein the access judging circuit prefetches data stored in the most probable address of the memory into the buffer memory before a memory access is carried out from the processor (C 7, L 32-46; C 10, L 19-50 - the access judging circuit accesses the memory and thus performs the prefetching operation in response to a read request from the prefetch request unit which is performed before a memory access is carried out from the processor).

Regarding claim 5, Tanabe discloses a plurality of buffers into which prefetched data is stored and wherein the control circuit transfers data in the buffer memories to the processor in an order different from an address order (sequentially) (Figure 17, References 38A-38D; C 13, L 51-55; C 16, L 50-53; each memory is accessed independently (in any order), thereby providing non-sequential data access).

Regarding claim 8, Tanabe discloses the control circuit in its initial state (state during a first time processor access request) to prefetch data already stored at a pre-specified address (address specified by the first processor access) into the buffer (C 7, L 28-52 – 32 bytes of data are

retrieved from the RDRAM into the prefetch buffer when a cache miss occurs wherein 16 bytes of the retrieved data are the requested data and the additional 16 bytes of data retrieved are the prefetched data).

Regarding claim 11, Tanabe discloses the processor comprising an internal cache (Figure 4, Reference 3a) and the control circuit is controlled to prefetch data having a data size of twice or more a line size of the internal cache (C 6, L 18-29; C 7, L 1-16). Tanabe discloses the line size of the internal cache as 16 bytes (C 5, L 26-28).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe (USPN: 5,752,272) in view of Genduso (USPN: 5,778,422).

Regarding claim 2, Tanabe discloses the limitations cited above in claim 1, and Tanabe discloses control circuitry (Figure 4, References 21 and 23) controlled to transfer data to the processor, when the access from the processor hits data within the buffer (C 7, L 52-67; C 8, L 1-3). However, Tanabe does not disclose a memory controller comprising a direct path (path excluding the buffer memory) for transmitting data directly to the processor from the memory there through, wherein the control circuit is controlled to transfer data within the memory to the

processor via the direct path when the access from the processor fails to hit data within the buffer memory. However, Genduso does teach a memory controller comprising a direct path (Figure 1, Reference 18) for transmitting data directly to the processor from the memory there through; wherein the control circuit (C 5, L 27-30), is controlled to transfer the data to the processor when the access from the processor hits data within the buffer memory (Figure 4, References 80-82, 88-90; C 6, L 11-20, L 24-31), and wherein the control circuit is controlled to transfer data within the memory to the processor via the direct path when the access from the processor fails to hit data within the buffer memory (Figure 4, Reference 110,112 and 108; C 6, L 49-60). One of ordinary skill in the art would have recognized the speed enhancement provided by transferring data to the processor from the memory controller via a direct path as taught by Genduso in comparison to Tanabe's method. In Tanabe's method the transferred data from the main memory is first stored in the buffer in the memory controller and then transferred to the processor from the buffer (C 7, L 40-52), which requires two data transfers instead of one, and additional control logic for managing both transfers and increased time. Therefore, it would have been obvious to one of ordinary skill in the art to use the teachings of Genduso in the system taught by Tanabe for the desirable purpose of improved performance and reduced latency.

13. Claim 3-4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe (USPN: 5,752,272) in view of Conary et al. (USPN: 5,935,253).

Regarding claims 3-4, Tanabe discloses prefetching information, however, Tanabe does not explicitly disclose prefetching instructions and data. However, Conary discloses prefetching

instructions and data (C 4, L 61-65). It is common knowledge that prefetching is performed to provide fast access to information requested by the processor. Processors access instructions and data from memory in performing tasks and thus prefetching instructions and data would be desirable to provide prompt access to the instructions and data thereby reducing memory latency and improving the performance of the system. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to prefetch instructions and data in Tanabe's system for the desirable purpose of reduced memory latency and improved performance.

14. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe (USPN: 5,752,272) in view of Genduso (USPN: 5,778,422), Lynch (USPN: 5,829,031) and Handy, The Cache Memory Book.

Regarding claim 12, Tanabe discloses the limitations cited above in claim 1, however, Tanabe does not disclose, the memory divided into a first memory for storing therein an instruction code to be executed on the processor and a second memory for storing therein operand data; wherein the memory controller has an access judgement circuit for judging whether the access from the processor is an access to the first memory or an access to the second memory, a first buffer memory for prefetching the instruction code and a second memory for prefetching of the operand data; wherein the control circuit is controlled to prefetch the instruction code into the first buffer memory according to a judgement of the access judgement circuit or to prefetch the operand data into the second buffer memory. However, Lynch discloses dividing a memory into a first memory for storing instructions (instruction cache) (Figure 1,

Reference 22) and a second memory for storing operand data (data cache)(Figure 1, Reference 24), wherein a memory controller (Figure 1, Reference 20 and cache controller, not shown – inherent, determines cache hit/miss) has an access judgement circuit (Figure 1, Reference 20) for judging whether the access from the processor is an access to the first memory or an access to the second memory (C 6, L 47-56). Handy teaches that this type of split cache (memory) architecture reduces thrashing, which improves the performance of the system, and is simple to construct (Page 60-61, Section titled Unified vs. Split Caches). Furthermore, this configuration is known in the art as a Harvard architecture, which improves the bandwidth of the system, when the memories are accessed independently by providing parallel access to each memory unit. Additionally, Genduso teaches the concept of a first buffer memory for prefetching instructions (Figure 2, Reference 44), a second buffer memory for prefetching data (Figure 2, Reference 46) and a controller (Figure 2, Reference 52) for prefetching instructions into the first buffer memory according to a judgement of an access judgement circuit (the circuitry/logic portion in the controller, which determines whether a processor access is an instruction request or a data request, Figure 3, C 5, L 36-67; C 6, L 1-64) or to prefetch data into the second buffer memory (C 8, L 51-67; C 9, L 1-67; C 10, L 1-7). As stated above, prefetching instructions and data improves the performance of the system by providing prompt access to information requested by the processor, which includes instructions and data. Tanabe teaches the use of one prefetch buffer, which may be subjected to thrashing issues, depending on what type of information is stored in the prefetch buffer. It would also be desirable to implement a Harvard architecture memory structure in Tanabe's system to increase the storage capacity and the bandwidth of the memory system. Thus it would have been obvious to one of ordinary skill in the art to use the

teachings of Lynch, Handy and Genduso with the system taught by Tanabe for the desirable purpose of improved performance.

15. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe (USPN: 5,752,272) in view of Suzuki (USPN: 5,381,532).

Tanabe discloses the limitations cited above in claim 1, however, Tanabe does not disclose the memory controller having an instruction decoder and a branching buffer, wherein the control circuit prefetches an instruction as a branch destination into the branching buffer when the instruction decoder detects a branch instruction and determining whether or not an instruction hits data within the buffer and the branching buffer when an access is made from the processor to the instruction. However, Suzuki discloses a memory controller (comprised of Figure 1, References 110, 150; Figure 2, entire) having an instruction decoder (Figure 2, Reference 130) and a branching buffer (Figure 2, Reference 201), wherein the control circuit (Figure 1, Reference 150, Figure 2, References 200, 202 and 205) prefetches an instruction as a branch destination into the branching buffer when the instruction decoder detects a branch instruction (C 5, L 38-40, L 46-58) and when an access is made from the processor to the instruction (branch taken) determining whether or not the instruction hits data within the buffer or the branching buffer (C 6, L 10-20 – the output of VTAKEN and UTAKEN determine whether the instruction is in the buffer or the branching buffer, when VTAKEN is active, the branch decoder outputs a high on signal 2021 in Figure 2, which allows the output of the branch buffer through the multiplexer to the instruction decoder and when the output of UTAKEN is high the output of the prefetch buffer is sent to the instruction decoder - C 6, L 62-66). Suzuki teaches that the above

features enhances prefetching and branch processing thereby improving the performance of the system (Abstract). Tanabe's system prefetches instructions and data sequentially from the requested address. If the processor executes a branch instruction, it is likely that the next instruction executed is not sequential to the branch instruction, unless the branch isn't taken. Therefore, the prefetched instructions will not be useful. Thus, it would have been obvious to one of ordinary skill in the art to use the teachings of Suzuki with the teachings of Tanabe for the desirable purpose of increasing the effectiveness of prefetching and improved performance.

16. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe (USPN:5,752,272) in view of Mirza (USPN: 5,357,618).

Tanabe discloses the limitations cited above in claim 1, however, Tanabe does not explicitly disclose the memory controller comprising a register for instructing start (enable) or stop (disable) of prefetch to the buffer memory. However, Mirza teaches the concept of starting (enabling) or stopping (disabling) prefetch operations to a buffer via a register (C 2, L 60-68; C 3, L 5-12). Mirza teaches memory access patterns are not always sequential and in such cases when prefetching is performed for sequential accesses the prefetch buffer/cache becomes polluted with data never referenced (C 1, L 36-68; C 2, L 1-33). Mirza's technique of selectively enabling and disabling prefetch operations optimizes the performance of the system by preventing prefetching for data stored at non-sequential (non-loop) access locations to prevent polluting the cache to reduce the cache miss rate. Tanabe's system seeks to reduce the cache miss rate by prefetching (C 14, L 21-25). Tanabe teaches that the cache miss rate can be reduced by the success of prefetch. The prefetch is successful when referenced data (non-polluted) is

retrieved via the prefetch operation. One of ordinary skill in the art at the time of the invention would have recognized the improved prefetch success rate afforded by Mirza's teachings and would have been motivated to use the teachings of Mirza with the teachings of Tanabe for the desirable purpose of improving the success rate of the prefetch operations and improving the performance of the system by reducing the cache miss rate.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo can be reached on 703-308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are 703-7467329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Kimberly N. McLean
Examiner
Art Unit 2187

KNM

March 22, 2002